Hot Operating Temperature Technology

Passively Compensated Low-Power Chip-Scale Clocks for Wireless Communication in Harsh Environments

Completed Technology Project (2017 - 2019)

Project Introduction

Stanford University in collaboration with JPL is proposing to develop an ultra-low power chip-scale timing unit that is the main building clock of any communicating system (analog or digital) to directly address the goals of the NASA HOTTech Program, which aims to mature high-temperature electrical and electronic systems for in-situ missions to harsh environments (Venus, Mercury or gas giants). The scientific data collected from any probe, lander, explorer, or sensor identified in the NASA decadal survey needs to be transferred to the main spacecraft in a robust fashion. Realizing a local oscillator or clock with a stable frequency output is the most crucial part of such a communication system and operation in extreme temperatures above 500C places new demands on such a critical component. The high-temperature chip-scale clock proposed here enables reduced thermal sensitivity at a wide range of temperatures, susceptibility to shock, and radiation effects. Such performance cannot be obtained from any other current, or planned product, with a solution that offers high science value through a small-size, low-weight, low-power (low SWaP), and, in the long-term, low-cost approach. The proposed system includes an array of three indium aluminum nitride (InAlN)/ gallium nitride (GaN) mechanical resonators with different temperature coefficients of frequency (TCFs), operating at their bulk resonance mode to achieve high thermal stability of < 1 ppm over the 470 to 530C range and acceleration survivability of >20,000 g without the need for high-power heaters. Our key innovation is the use of wide bandgap nanofabrication technology to implement passively compensated resonators with zero-bias TCF of sub-ppm levels at and around 500C. Further, these resonators offer a high Q of more than 5,000 and small motional impedance and can be monolithically integrated with high-temperature III-V amplifiers - all characteristics required for achieving low-phase noise and low-power clocks. InAlN/GaN high electron mobility transistors are proven to be operable up to 1000C and resonators in GaN and other III-Vs are shown to offer high-temperature operation, high power stability, high Q, and designable zero-bias TCF values in a wide temperature range (up to 600C). In this program, we will integrate the resonators in an array and multiplex their output to get a final frequency readout with an accuracy that is 260 times better than that of a single resonator clock and functional at 500C. The design and implementation of the chip-scale clock has an entry technology readiness level (TRL) of 2 and exit TRL of 4. It should also be noted that this work readily translates to commercial ground-based applications such as oil and gas, geothermal and combustion.

Anticipated Benefits

An in-situ lander to Venus was solicited as one of seven possible new frontiers missions in 2017, and the Venus Exploration and Analysis Group (VEXAG) has outlined four possible missions (mid- and far- term) that require lander operation of the surface of Venus. If any of these missions went

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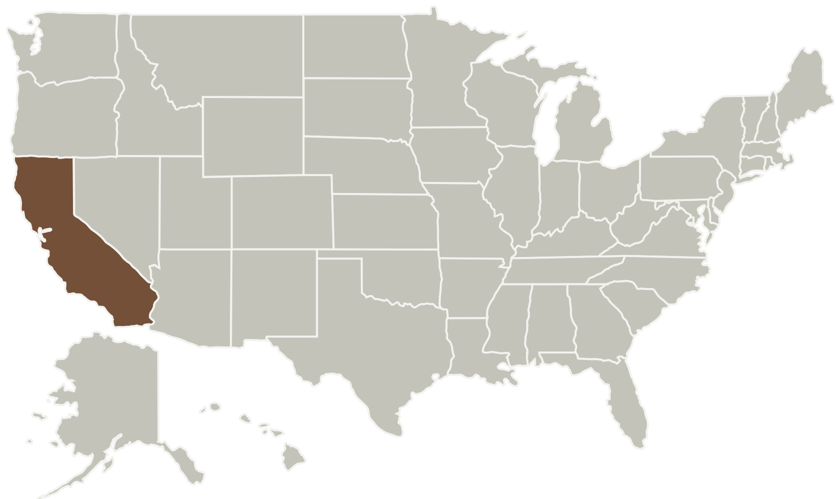
Table of Contents

forward, high-temperature capable communication would be required, and this technology develops a temperature-stable oscillator integral stable collection/transmission/communication of scientific data.

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Stanford University(Stanford)	Lead Organization	Academia	Stanford, California

Primary U.S. Work Locations
California

Organizational Responsibility

Responsible Mission Directorate:

Science Mission Directorate (SMD)

Lead Organization:

Stanford University (Stanford)

Responsible Program:

Hot Operating Temperature Technology

Project Management

Program Director:

Carolyn R Mercer

Program Manager:

Quang-viet Nguyen

Principal Investigator:

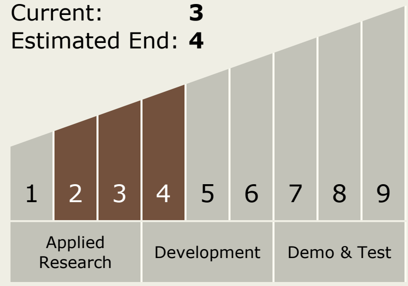
Debbie Senesky

Co-Investigators:

Mina Rais-zadeh
Natalie M Muzzio

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **4**



Technology Areas

Primary:

- TX05 Communications, Navigation, and Orbital Debris Tracking and Characterization Systems
  - └ TX05.4 Network Provided Position, Navigation, and Timing
    - └ TX05.4.1 Timekeeping and Time Distribution

Target Destination

Others Inside the Solar System